APEX SEMICONDUCTOR
Analog & Mixed-Signal Solutions

ADX2050

Dual-Channel Precision, Low-Noise Operational Amplifier

Doc. No.	APX-ADX2050-DS
Revision	C
Date	2026-06-15
Class.	Public
ECCN	EAR99

1 General Description

The ADX2050 is a dual-channel, precision operational amplifier optimized for low-noise, low-offset signal conditioning in industrial and instrumentation applications. Fabricated on Apex Semiconductor's third-generation complementary bipolar process, the ADX2050 combines rail-to-rail output swing with a wide 3 V to 32 V single-supply operating range, enabling direct interfacing with sensor bridges, thermocouples, and precision data-acquisition front ends.

Each amplifier channel is unity-gain stable and offers a 10 MHz gain-bandwidth product with a 5.5 V/µs slew rate, making the device well suited to active filtering and moderate-speed signal-processing tasks. The ADX2050 is offered in an 8-pin SOIC package and is fully specified over the $-40\,^{\circ}\mathrm{C}$ to $+125\,^{\circ}\mathrm{C}$ industrial temperature range.

2 Features

- Ultra-low input offset voltage: 0.3 mV (typ), 1.2 mV (max)
- Low input bias current: 45 nA (typ)
- Wide supply range: 3 V to 32 V single-supply, ±1.5 V to ±16 V dual-supply
- Rail-to-rail output swing
- Unity-gain stable, 10 MHz gain-bandwidth product
- Low voltage noise density: $8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 kHz
- Industrial temperature range: $-40\,^{\circ}\mathrm{C}$ to $+125\,^{\circ}\mathrm{C}$
- ESD protection: 2 kV (HBM), 1 kV (CDM)
- Available in 8-pin SOIC package

3 Applications

- Precision instrumentation amplifiers
- Sensor and bridge signal conditioning
- Battery-powered and portable medical instrumentation
- Audio pre-amplification
- Industrial process-control loops (4–20 mA)
- Active filters and signal buffering

© 2026 Apex Semiconductor, Inc.

4 Pin Configuration and Functions

4.1 Pinout Diagram

Figure 1. ADX2050 pin configuration, 8-pin SOIC package (top view). Pin 1 is marked by the reference dot.

4.2 Pin Description

Table 1. Pin functions.

Pin	Name	Type	Description
1	OUT1	Output	Output of amplifier channel 1
2	IN1–	Input	Inverting input, channel 1
3	IN1+	Input	Non-inverting input, channel 1
4	V–	Power	Negative supply / ground (single-supply operation)
5	IN2+	Input	Non-inverting input, channel 2
6	IN2–	Input	Inverting input, channel 2
7	OUT2	Output	Output of amplifier channel 2
8	V+	Power	Positive supply

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only; functional operation at or beyond these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings ($T_A = 25\,^{\circ}\mathrm{C}$ unless otherwise noted).

© 2026 Apex Semiconductor, Inc.

Parameter	Symbol	Rating	Unit
Supply voltage (V+ to V–)	V_S	-0.3 to 36	V
Differential input voltage	V_{ID}	± 36	V
Input voltage (either input)	V_{IN}	(V–)-0.3 to (V+)$+0.3$	V
Output short-circuit duration	–	Continuous	–
Continuous power dissipation	P_D	Internally limited	–
Junction temperature	T_J	150	°C
Storage temperature range	T_{STG}	-65 to 150	°C
Lead temperature (soldering, 10 s)	T_L	260	°C
ESD rating, human body model	–	2000	V
ESD rating, charged device model	–	1000	V

ESD Sensitivity. This device contains circuitry sensitive to electrostatic discharge (ESD). Apex Semiconductor recommends that proper ESD precautions be observed during handling, storage, and assembly to prevent damage or parametric degradation.

6 Recommended Operating Conditions

Table 3. Recommended operating conditions.

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage, single-supply	V_S	3.0	5.0	32	V
Supply voltage, dual-supply	$V_{S\pm}$	± 1.5	± 5.0	± 16	V
Operating free-air temperature	T_A	-40	25	125	°C
Common-mode input voltage range	V_{ICR}	(V–)	–	(V+)-1.5	V

7 Electrical Characteristics

7.1 DC Characteristics

Unless otherwise noted: $V_S = 5\,\text{V}$, $T_A = 25\,°\text{C}$.

Table 4. DC electrical characteristics.

© 2026 Apex Semiconductor, Inc.

Parameter	Sym.	Test Conditions	Min	Typ	Max	Unit
Input offset voltage	V_{OS}	$V_{CM} = V_S/2$	–	0.3	1.2	mV
Input offset voltage drift	$\Delta V_{OS}/\Delta T$	–	–	2	8	µV/°C
Input bias current	I_B	–	–	45	150	nA
Input offset current	I_{OS}	–	–	5	40	nA
Common-mode rejection ratio	CMRR	$V_{CM} = 0$ to 3 V	85	100	–	dB
Power-supply rejection ratio	PSRR	$V_S = 3$ V to 32 V	90	108	–	dB
Large-signal voltage gain	A_{VOL}	$R_L = 10\,\text{k}\Omega$, $V_O = 0.5$ to 4.5 V	100	120	–	dB
Output voltage, high	V_{OH}	$R_L = 10\,\text{k}\Omega$ to $V_S/2$	$V_S{-}0.15$	$V_S{-}0.05$	–	V
Output voltage, low	V_{OL}	$R_L = 10\,\text{k}\Omega$ to $V_S/2$	–	0.03	0.15	V
Output short-circuit current	I_{SC}	–	15	25	–	mA
Supply current (per amplifier)	I_{CC}	No load	–	0.6	0.9	mA

Typical values represent the most likely parametric norm at $T_A = 25\,^\circ$C and are not production tested. Min/Max limits apply over the full recommended operating temperature range unless otherwise noted.

7.2 AC / Switching Characteristics

Unless otherwise noted: $V_S = 5$ V, $T_A = 25\,^\circ$C, $C_L = 100$ pF.

Table 5. AC and switching characteristics.

Parameter	Sym.	Test Conditions	Min	Typ	Max	Unit
Gain-bandwidth product	GBW	–	–	10	–	MHz
Slew rate	SR	$R_L = 2\,\text{k}\Omega$	–	5.5	–	V/µs
Phase margin	ϕ_m	$C_L = 100$ pF	–	60	–	deg
Settling time (0.1%)	t_S	2 V step	–	1.2	–	µs
Total harmonic distortion+noise	THD+N	$f = 1$ kHz, $A_V = 1$	–	0.002	–	%
Input voltage noise density	e_n	$f = 1$ kHz	–	8	–	nV/$\sqrt{\text{Hz}}$
Input current noise density	i_n	$f = 1$ kHz	–	0.3	–	pA/$\sqrt{\text{Hz}}$
Channel separation	–	$f = 1$ kHz	100	120	–	dB

8 Package Mechanical Data

The ADX2050 is supplied in an industry-standard 8-pin small outline (SOIC-8) package, illustrated in Figure 2. Dimensions are per Table 7.

© 2026 Apex Semiconductor, Inc.

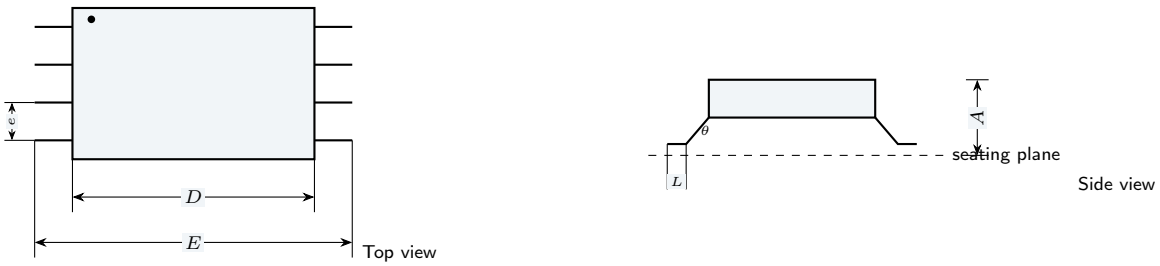

Figure 2. SOIC-8 package outline, top and side views (schematic, not to scale).

Table 6. Package mechanical dimensions.

Symbol	Min	Nom	Max	Unit
A	–	–	1.75	mm
A_1	0.10	–	0.25	mm
A_2	1.25	1.45	1.65	mm
b	0.31	–	0.51	mm
c	0.17	–	0.25	mm
D	4.80	4.90	5.00	mm
E	5.80	6.00	6.20	mm
E_1	3.80	3.90	4.00	mm
e	–	1.27 BSC	–	mm
L	0.40	–	1.27	mm
θ	0	–	8	deg

9 Ordering Information

Table 7. Ordering information.

Order Part No.	Temp. Range	Package	Marking	Transport Media
ADX2050AIDR	-40 to $125\,^{\circ}$C	SOIC-8 (D)	ADX2050A	Tape and reel, 2500 units
ADX2050AID	-40 to $125\,^{\circ}$C	SOIC-8 (D)	ADX2050A	Rails, 100 units/rail
ADX2050ACDR	0 to $70\,^{\circ}$C	SOIC-8 (D)	ADX2050AC	Tape and reel, 2500 units

All package types comply with JEDEC MS-012 and are RoHS-compliant / halogen-free.

10 Symbols and Abbreviations

Table 8. Symbols and abbreviations used in this document.

© 2026 Apex Semiconductor, Inc.

Symbol	Definition
V_{OS}	Input offset voltage
I_B	Input bias current
I_{OS}	Input offset current
CMRR	Common-mode rejection ratio
PSRR	Power-supply rejection ratio
GBW	Gain-bandwidth product
SR	Slew rate
THD+N	Total harmonic distortion plus noise
ESD	Electrostatic discharge
HBM	Human body model
CDM	Charged device model
T_A	Ambient temperature
T_J	Junction temperature
RoHS	Restriction of Hazardous Substances (Directive 2011/65/EU)
BSC	Basic spacing between centers (theoretically exact dimension)

11 Revision History

Table 9. Document revision history.

Rev	Date	Description	Approved
A	2025-11-03	Initial release.	J. Alvarez
B	2026-02-18	Updated AC characteristics; corrected pin-1 orientation in Figure 1.	J. Alvarez
C	2026-06-15	Added industrial temperature grade; revised Ordering Information (Table 8).	M. Chen

Important Notice. This document contains information on a product under continuing development. Apex Semiconductor, Inc. reserves the right to change or discontinue this product without notice. Apex Semiconductor does not assume any liability arising out of the application or use of this product. All trademarks are the property of their respective owners.