High-Speed Processor Board

Project Apex-X – PCB Design Document

Synapse Robotics Inc. | Hardware Engineering Group

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Revision: 2.1
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Author: Sarah Jenkins

1 Document Revision History

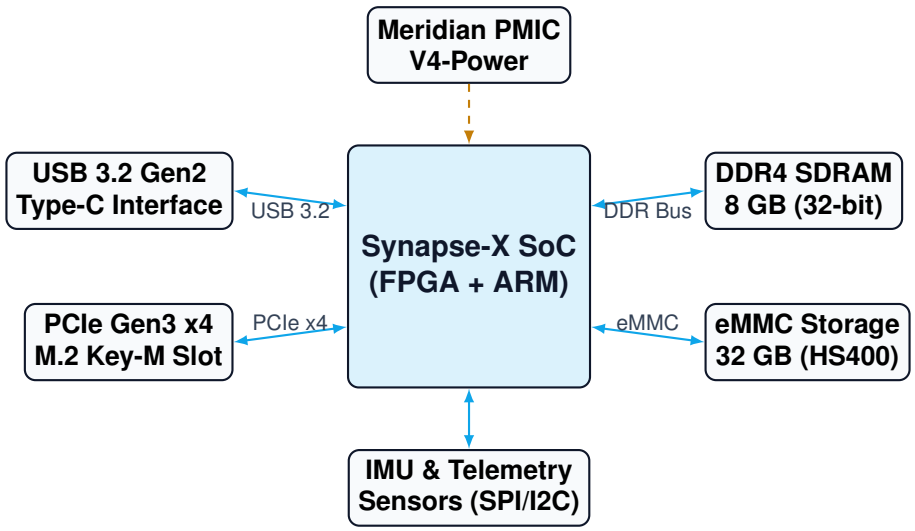
This design document defines the physical layout rules, schematic integration guidelines, stackup configurations, and routing requirements for the Project Apex-X processor board. All modifications must be tracked and approved by the Hardware Engineering Group.

Revision	Date	Author	Description of Changes
1.0	Jan 12, 2026	Sarah Jenkins	Initial draft for schematic entry and footprint validation.
1.1	Mar 05, 2026	Sarah Jenkins	Added DDR4 impedance profile and updated decoupling rules.
2.0	May 20, 2026	Sarah Jenkins	Updated stackup to 6-layer structure for signal integrity optimization.
2.1	Jul 15, 2026	Sarah Jenkins	Final release for pre-production fabrication. Added PCIe lane rules.

Table 1: Document Revision Log

2 System Overview & Block Diagram

The Project Apex-X processor board acts as the central controller for high-speed edge computing applications. It relies on the Synapse-X SoC, which integrates FPGA fabric with quad-core ARM processing units, flanked by DDR4 SDRAM and eMMC storage.

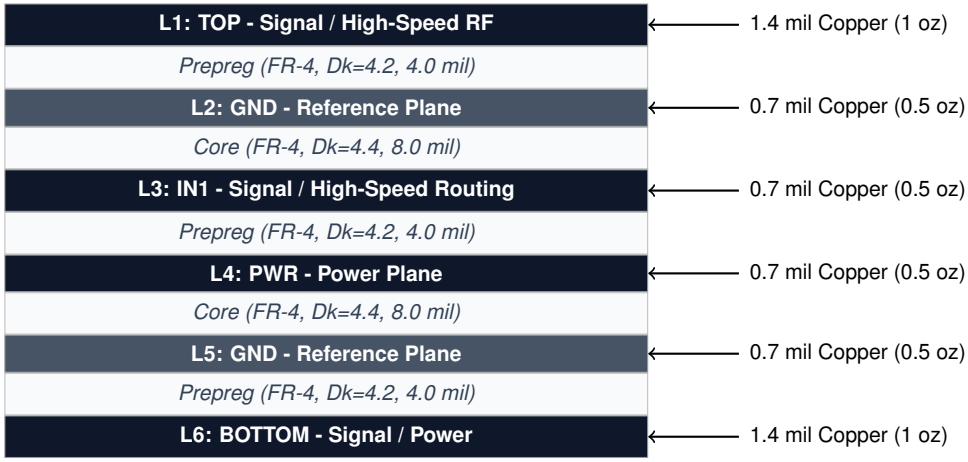


3 PCB Layer Stackup & Physical Parameters

The design utilizes a 6-layer stackup to optimize signal routing, shield critical nets, and distribute power. This structure provides dedicated reference planes directly adjacent to every signal routing layer.

3.1 Stackup Diagram

The physical construction of the board is outlined below. Layer thicknesses have been selected to ensure an overall nominal thickness of 62 mils (1.6 mm).



3.2 Stackup Specifications

Table 2 details the layer properties. The dielectric constant (Dk) is specified at 1 GHz.

Layer	Name	Type	Material	Thickness	Dk	Copper Wt
-	Solder Mask	Dielectric	Liquid Photo Imageable	0.8 mil	3.5	-
1	TOP	Signal	Copper Foil / FR-4	1.4 mil	4.2	1.0 oz
-	Prepreg	Dielectric	FR-4 2116	4.0 mil	4.2	-
2	GND	Plane	Copper Foil / FR-4	0.7 mil	4.4	0.5 oz
-	Core	Dielectric	FR-4 Core	8.0 mil	4.4	-
3	IN1	Signal	Copper Foil / FR-4	0.7 mil	4.2	0.5 oz
-	Prepreg	Dielectric	FR-4 2116	4.0 mil	4.2	-
4	PWR	Plane	Copper Foil / FR-4	0.7 mil	4.4	0.5 oz
-	Core	Dielectric	FR-4 Core	8.0 mil	4.4	-
5	GND	Plane	Copper Foil / FR-4	0.7 mil	4.4	0.5 oz
-	Prepreg	Dielectric	FR-4 2116	4.0 mil	4.2	-
6	BOTTOM	Signal	Copper Foil / FR-4	1.4 mil	4.2	1.0 oz
-	Solder Mask	Dielectric	Liquid Photo Imageable	0.8 mil	3.5	-

Table 2: Detailed Layer Parameter Table

4 Routing Rules & Impedance Control

To prevent signal reflections and cross-talk, controlled impedance is required on all high-speed signals. Signal paths must comply with the target geometries outlined in Table 3.

Interface	Target Impedance	Trace Width (w)	Spacing (s)	Reference Layers
Single-Ended Reference	50 $\Omega \pm 10\%$	4.5 mil	-	L2 (GND), L5 (GND)
USB 2.0 / 3.2 Diff Pair	90 $\Omega \pm 10\%$	4.0 mil	5.0 mil	L2 (GND), L5 (GND)
PCIe Gen3 Lanes	100 $\Omega \pm 10\%$	3.8 mil	6.0 mil	L2 (GND)
DDR4 Diff Clock	100 $\Omega \pm 10\%$	3.8 mil	5.5 mil	L2 (GND), L5 (GND)
DDR4 Data / Address	40 Ω single-ended	5.2 mil	-	L2 (GND), L5 (GND)

Table 3: Impedance Control Target Parameters

High-Speed Routing Best Practices

- **Reference Planes:** High-speed differential pairs must run continuously over an uninterrupted ground reference plane (L2 or L5). Avoid routing across splits or voids.
- **Via Count:** Limit via count on high-speed paths (PCIe, USB 3.2) to a maximum of two. Each via transition must have an adjacent ground return via placed within 15 mils.
- **Length Matching:** USB 3.2 Rx/Tx differential pairs must be length-matched within $\pm$ 5 mils. DDR4 data lanes within the same byte lane must be length-matched within $\pm$ 10 mils.

5 Power Delivery Network (PDN) Guidelines

The design includes multiple power rails generated by the PMIC. Table 4 summarizes the target voltage, maximum expected current, ripple tolerance, and routing requirements for each rail.

Rail Name	Voltage	Max Current	Ripple Limit	Routing Topology
VCC_3V3	3.3 V	2.0 A	$\pm$ 5%	Star topology, minimum 40 mil trace width.
VCC_1V8	1.8 V	1.5 A	$\pm$ 5%	Power plane routing on L4.
VCC_1V2_DDR	1.2 V	4.0 A	$\pm$ 3%	Solid copper pour on L4, decouple with 0.1 μF.
VCC_0V85_SoC	0.85 V	12.0 A	$\pm$ 2%	Dedicated plane cavity, multipoint capacitor connections.
VDD_VTT	0.6 V	1.0 A	$\pm$ 5%	Trace routing adjacent to DDR4 address bus.

Table 4: Power Supply Rail Performance Requirements

6 Pre-Release Layout Checklist

Before exporting manufacturing Gerber files, layout design rules must be validated against the manufacturing checklist below.

[ ] Verify that all 50 Ω single-ended traces match width constraints.

[ ] Verify that return vias are placed next to high-speed signal vias.

[ ] Confirm PMIC power trace widths satisfy current requirements (minimum 20 mil width per 1A).

[ ] Ensure decoupling capacitors are placed directly at the pin entry points.

[ ] Run complete DRC check in Altium and verify zero violations.