Vertex-9 FPGA DSP Accelerator

High-Performance Signal Processing Core Design Specification

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Revision History

Version	Date	Description	Author
1.0.0	Oct 12, 2025	Initial architecture draft for review.	S. Jenkins
2.0.0	Feb 18, 2026	Added multi-channel DMA support.	R. Patel
2.3.0	May 05, 2026	Refined clock domain crossing (CDC) constraints.	J. Carter
2.4.0	Jul 15, 2026	Updated register map and DSP timing parameters.	S. Jenkins

1 Executive Summary

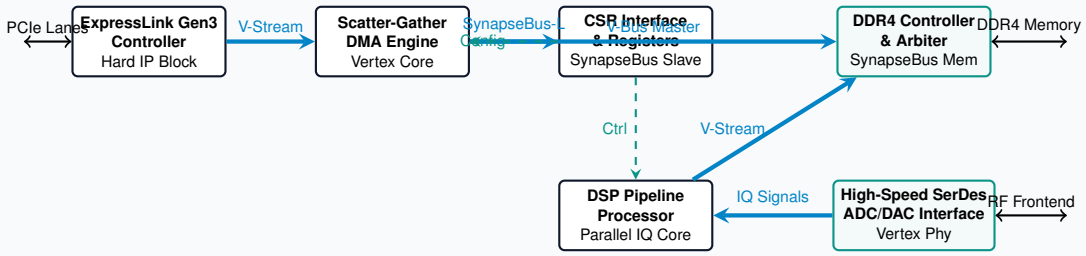
This document defines the architectural, functional, and physical interface specifications for the Vertex-9 High-Performance DSP FPGA Accelerator core. Developed by Vertex Systems, the Vertex-9 is a modular, high-throughput signal processing engine tailored for multi-channel RF transceiver systems.

The core integrates an ExpressLink Gen3 x4 PCIe host interface, a dual-channel scatter-gather DMA engine, a configurable control and status register (CSR) file, and a pipelined DSP processor optimized for parallel IQ filtering. The target implementation platforms are Nexa-Gate Ultra 900 and Meridian-7 series FPGAs, delivering deterministic latency and high spectral efficiency under strict power constraints.

2 System Architecture

The Vertex-9 core architecture utilizes a decoupled design topology, isolating the host interface domain from the high-frequency DSP processing pipelines. All system control, DMA configuration, and signal parameters are governed by the control and status register file.

Figure 1: Internal FPGA Architecture Block Diagram



2.1 Core Subsystem Descriptions

- **ExpressLink Gen3 Controller:** Fictional hard macro handling physical, link, and transaction layer protocols for host interfacing. Bridges standard system PCIe commands to internal protocols.
- **Scatter-Gather DMA Engine:** Dedicated controller designed to support ring-buffered, non-contiguous host memory access. Coordinates dual-channel memory-mapped transfers to and from DDR4 RAM.
- **Control & Status Registers (CSR):** Interconnect endpoints accessed via the SynapseBus-Lite register protocol. Manages hardware parameter configuration and reports processing health.
- **DSP Pipeline Processor:** Fixed-point signal processor consisting of parallel multiply-accumulate (MAC) arrays and circular pipeline registers.

3 Register Map (CSR Interface)

The control and status register block is accessed via a 32-bit SynapseBus-Lite interface. All registers are 32 bits wide and aligned to 4-byte boundaries.

Offset	Register Name	Access	Reset Value	Description
0x0000	CTRL_REG	R/W	0x00000000	Global Control Register. Controls core enabling, resets, and operational modes.
0x0004	STATUS_REG	R/O	0x00000001	Global Status Register. Exposes FIFO flags, processing status, and errors.
0x0008	INTR_EN	R/W	0x00000000	Interrupt Enable Register. Enables hardware interrupt sources.
0x000C	INTR_STAT	R/W1C	0x00000000	Interrupt Status Register. Write '1' to clear active interrupt signals.
0x0010	DMA_SRC_ADDR	R/W	0x00000000	DMA Source Base Address (Lower 32-bits).
0x0014	DMA_DST_ADDR	R/W	0x00000000	DMA Destination Base Address (Lower 32-bits).
0x0018	DMA_LENGTH	R/W	0x00000000	DMA Transfer Length in bytes. Writing triggers transfer.
0x0020	DSP_PARAM_A	R/W	0x00004000	DSP Filter Coefficient A (1.15 fixed-point format).
0x0024	DSP_PARAM_B	R/W	0x00007FFF	DSP Filter Coefficient B (1.15 fixed-point format).

3.1 Control Register Field Descriptions (CTRL_REG)

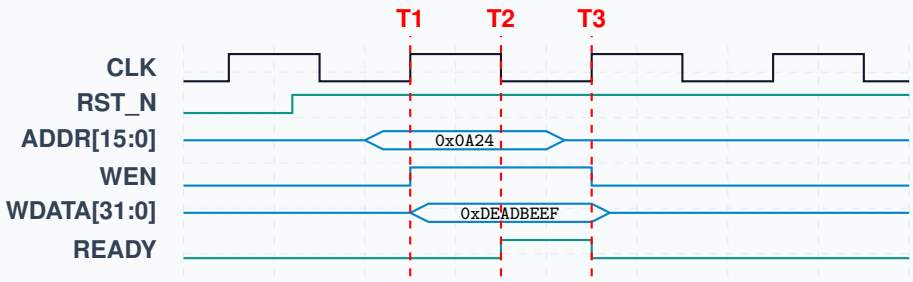
The CTRL_REG controls the general operation of the Vertex-9 DSP core.

Bits	Field Name	Access	Reset	Field Description
31:16	*Reserved*	R/O	0x0000	Reserved for future expansion. Reads return 0.
15:8	`DSP_MODE`	R/W	0x00	Selects processing algorithm: 0x00 (Bypass), 0x01 (FIR Filter), 0x02 (FFT Mode), 0x03 (Correlator).
7:4	*Reserved*	R/O	0x0	Reserved for future expansion. Reads return 0.
3	`INTR_EN_GL`	R/W	0x0	Global Interrupt Enable. Active high.
2	`SOFT_RST`	R/W	0x0	Software Reset. Write '1' to reset the DSP pipeline. Self-clearing.
1	`RUN`	R/W	0x0	Run Enable. Write '1' to start data processing.
0	`CORE_EN`	R/W	0x0	Global Core Enable. Must be '1' for any sub-modules to operate.

4 Interface Protocols & Timing Handshake

The SynapseBus-Lite interface utilizes a strict handshaking interface. The master asserts the write enable (`WEN`) and supplies address and data. The slave core asserts the `READY` signal to indicate that the write operation has been accepted and registered.

Figure 2: CSR Write Transaction Timing Handshake



4.1 Write Transaction Sequence

1. **Time T1:** The bus master drives the write address (`0x0A24`) and write enable (`WEN`) signals. The write data bus (`WDATA`) becomes valid with the value `0xDEADBEEF`.
2. **Time T2:** The slave core decodes the address and asserts `READY` on the falling edge of the clock cycle, signaling that it is prepared to register the transaction.
3. **Time T3:** On the next rising edge of the system clock, the write operation is committed, data is latched into the target CSR, and the master de-asserts `WEN` to conclude the write transaction.

5 Physical Implementation & Resource Summary

The Vertex-9 core features isolated clock domains to optimize maximum speed paths. Hardware compilation properties are defined below.

5.1 Clock Domain and Reset Strategy

The logic structure relies on three distinct clock domains to prevent timing violation paths:

- **System Clock (`sys_clk`):** Operates at 250 MHz. Used for DMA controller logic and the ExpressLink physical link layer interface.
- **Configuration Clock (`cfg_clk`):** Operates at 100 MHz. Used for low-speed CSR read/write access.
- **Core DSP Clock (`dsp_clk`):** Runs at 400 MHz. Dedicated to parallel processing arithmetic.

Asynchronous Clock Domain Crossings (CDC) are isolated using dual-clock FIFOs and dual-flip-flop synchronizers.

Synthesis Directives

- **FSM Encoding:** One-Hot
- **Resource Sharing:** Disabled
- **DSP Mapping:** Block RAM limit
- **Logic Optimization:** Retiming
- **Boundary Keep:** False

Place & Route Constraints

- **Placement Strategy:** High-Speed
- **Routing Effort:** Maximum
- **Physical Optimization:** Enabled
- **Hold-Time Fix:** Aggressive
- **Slack Threshold:** 0.05 ns

5.2 Hardware Resource Utilization Metrics

Utilization is estimated based on compilation targeting default parameter options.

Target Device	LUTs	Flip-Flops	BRAM (36Kb)	DSP Slices	F_{max} (MHz)
Nexa-Gate Ultra 900	12,450 (2.4%)	18,900 (1.8%)	45 (4.2%)	128 (6.7%)	450 MHz
Meridian-7 F-Series	10,800 (1.9%)	16,500 (1.5%)	38 (3.5%)	128 (5.8%)	520 MHz

5.3 Physical Top-Level Pin Constraints

Port Name	Direction	Width	IO Standard	Description
`pcie_rx_p/n`	Input	4	`DIFF_SSTL12`	PCIe Differential Receive Lanes.
`pcie_tx_p/n`	Output	4	`DIFF_SSTL12`	PCIe Differential Transmit Lanes.
`sys_clk_p/n`	Input	1	`LVDS`	Reference Clock for ExpressLink PLL.
`adc_data_in`	Input	14	`LVDS_25`	Differential ADC data inputs from SerDes.
`dac_data_out`	Output	14	`LVDS_25`	Differential DAC data outputs to SerDes.
`sys_rst_n`	Input	1	`LVCMOS18`	Active Low Global Asynchronous Reset.