Solstice Semiconductor APPLICATION NOTE

5V-to-3.3V, 2A Synchronous Buck Converter Reference Design for Industrial IoT Sensor Nodes

Featuring the SSC61830 Synchronous Buck Converter Controller

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Revision History

Rev	Date	Author	Description of Change
A	2025-11-03	D. Alvarez	Initial release.
B	2026-02-18	D. Alvarez	Updated bill of materials for X7R dielectric substitution; added thermal derating note.
C	2026-06-15	M. Chen	Added oscilloscope validation data; revised feedback divider values for tighter output-voltage tolerance.

1 Scope

This application note describes a complete reference design for a 5 V-to-3.3 V, 2 A synchronous buck converter intended to power sensor and communication subsystems in industrial Internet-of-Things (IoT) nodes. It covers the circuit design, component selection with trade-off rationale, printed-circuit-board (PCB) layout guidance, and bench validation results for a design built around the Solstice Semiconductor SSC61830 synchronous buck converter controller.

This document does *not* cover firmware, digital communication interfaces, or enclosure/mechanical design. Full electrical specifications for the SSC61830 are provided in the associated datasheet, Reference 1.

2 Symbols, Abbreviations, and Acronyms

V_{IN}	Input supply voltage
V_{OUT}	Regulated output voltage
I_{OUT}	Output load current
f_{SW}	Switching frequency
D	Duty cycle
ΔV_{OUT}	Output voltage ripple (peak-to-peak)
η	Power conversion efficiency
ESR	Equivalent series resistance
EMI	Electromagnetic interference
PWM	Pulse-width modulation
SMD	Surface-mount device
PCB	Printed circuit board
RMS	Root mean square
ECO	Engineering change order

3 System Overview and Design Requirements

Industrial IoT sensor nodes are commonly powered from a 5 V USB or wall-adapter rail and require a well-regulated 3.3 V supply for microcontrollers, radios, and analog front ends. The converter must remain efficient across a wide load range, tolerate the ambient temperature extremes of an outdoor enclosure, and keep switching-noise coupling to a minimum so nearby analog sensor channels are not disturbed.

3.1 Functional Requirements

REQ-1: The regulator shall accept an input voltage range of 4.5 V to 5.5 V.

REQ-2: The regulator shall deliver a regulated output of 3.3 V ±2% at up to 2 A continuous load current.

REQ-3: Efficiency shall exceed 90% at 1 A load, 5 V input.

REQ-4: Output voltage ripple shall not exceed 33 mV peak-to-peak (1% of V_{OUT}) at full load.

REQ-5: The design shall operate over an ambient temperature range of -40°C to $+85$°C.

REQ-6: Quiescent supply current in light-load operation shall not exceed 25 µA.

REQ-7: Conducted EMI emissions shall comply with CISPR 32 Class B limits, Reference 3.

3.2 Target Applications

- Battery-backed industrial IoT sensor nodes
- Distributed PLC digital and analog I/O modules
- Low-power edge gateways and wireless sensor hubs

4 Circuit Description

4.1 Power Stage

The power stage uses the SSC61830, a peak-current-mode synchronous buck converter controller with integrated 30 V / 2.5 A high-side and low-side MOSFETs. The controller switches at a fixed frequency of 500 kHz, set internally, and regulates the output through an external resistive feedback divider. Figure 1 shows the simplified schematic of the power stage.

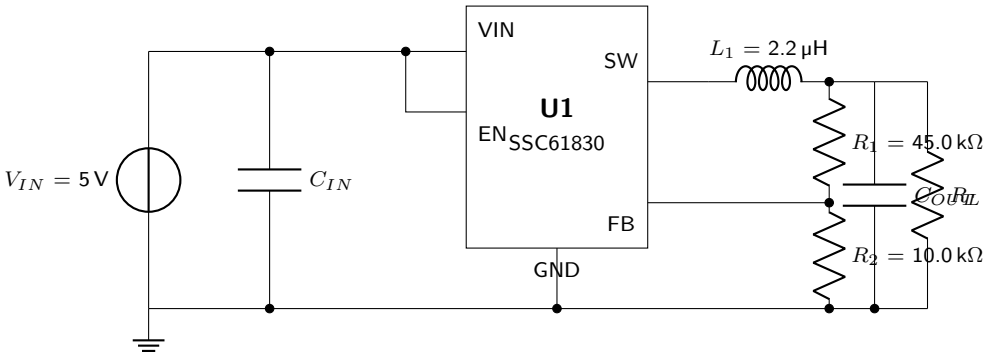


Figure 1: Simplified schematic of the 5 V-to-3.3 V, 2 A synchronous buck converter built around the SSC61830 controller.

4.2 Feedback Network Design

The SSC61830 regulates its feedback (FB) pin to an internal reference, $V_{REF} = 0.6\,\text{V}$. The output voltage is set by the resistive divider R_1, R_2 according to:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

Choosing $R_2 = 10.0\,\text{k}\Omega$ (a divider current of approximately 60 µA) and solving Equation (1) for a 3.3 V output gives $R_1 = 45.0\,\text{k}\Omega$. Both resistors use 1% tolerance thin-film parts to hold the output within the $\pm 2\%$ requirement of REQ-2 across process and temperature.

5 Bill of Materials

Table 1 lists the components used in the reference design shown in Figure 1.

Ref. Des.	Description	Value	Package	Mfr. Part Number	Qty
U1	Synchronous buck converter controller	SSC61830	HTSSOP-16	Solstice SSC61830QTR	1
L1	Shielded power inductor	2.2 µH, 4.5 A sat.	4x4x1.8 mm	Coilcraft XAL4020-222	1
Cin	X7R ceramic capacitor	10 µF, 10 V	0805	Murata GRM21BR61A106KE19L	2
Cout	X7R ceramic capacitor	22 µF, 6.3 V	0805	Murata GRM21BR60J226ME39L	2
R1	Thin-film resistor, 1%	45.0 kΩ	0402	Yageo RC0402FR-0745K0L	1
R2	Thin-film resistor, 1%	10.0 kΩ	0402	Yageo RC0402FR-0710KL	1
R_{EN}	EN pull-up resistor	100 kΩ, 5%	0402	Yageo RC0402JR-07100KL	1
C_{FF}	Feed-forward capacitor (optional)	10 pF, 50 V	0402	TDK C1005C0G1H100J	1

Table 1: Reference design bill of materials.

6 Design Trade-off Analysis

6.1 Inductor Selection

Table 2 compares the selected 2.2 µH inductor against a higher-inductance alternative.

Parameter	2.2 µH (Selected)	4.7 µH (Alternate)	Design Impact
Peak-to-peak ripple current	1.15 A	0.54 A	Lower L raises conduction loss slightly but improves load-transient slew rate.
Output voltage ripple	28 mV	14 mV	Higher L reduces ripple, easing the REQ-4 margin further.
Solution footprint	4x4x1.8 mm	5x5x2.0 mm	Smaller part saves approximately 2.4 mm^2 of board area.
Efficiency at 1 A	91.2%	92.6%	Higher L gives a modest efficiency gain from lower RMS current.
Recommendation	2.2 µH selected to prioritize fast load-transient response for sensor wake events over the small efficiency gain of the larger part.		

Table 2: Inductor value trade-off analysis.

6.2 Switching Frequency Selection

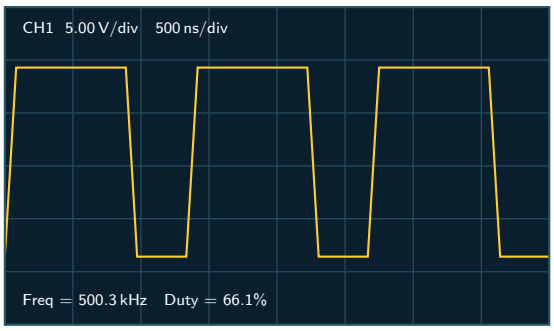
Table 3 summarizes the trade-off between the selected 500 kHz switching frequency and a 1 MHz alternative.

Parameter	500 kHz (Selected)	1 MHz (Alternate)	Design Impact
Passive component size	Larger L_1, C_{OUT}	Smaller L_1, C_{OUT}	1 MHz permits a smaller solution footprint.
Switching loss	Lower	Higher	500 kHz reduces gate-drive and switching losses, favoring efficiency.
Conducted EMI	Lower peak, easier filtering	Higher fundamental frequency	500 kHz was selected for margin against the REQ-7 CISPR 32 Class B limit.

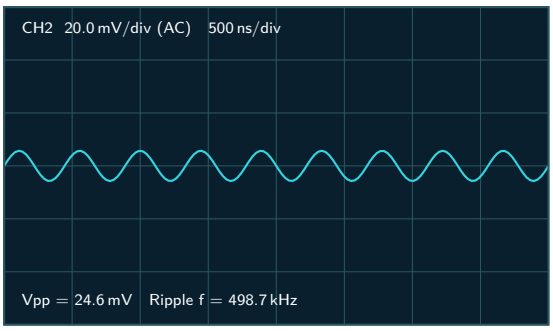
Table 3: Switching frequency trade-off analysis.

7 Bench Validation

The reference design was built and measured on the bench under the conditions of Section 3.1. Figure 2 shows representative oscilloscope captures of the switch-node waveform and the output ripple voltage at $V_{IN} = 5\,\text{V}$, $I_{OUT} = 2\,\text{A}$.



(a) *Switch-node (SW) voltage*



(b) V_{OUT} *ripple, AC-coupled*

Figure 2: Representative bench oscilloscope captures at $V_{IN} = 5\,\text{V}$, $I_{OUT} = 2\,\text{A}$. Waveforms are illustrative placeholders for the captured screen data.

Table 4 summarizes key measured parameters against the requirements of Section 3.1.

Parameter	Test Condition	Measured	Spec	Result
Efficiency	$V_{IN} = 5\,\text{V}$, $I_{OUT} = 1\,\text{A}$	91.4%	>90%	Pass
V_{OUT} accuracy	$I_{OUT} = 0$ to 2 A	3.29 V – 3.31 V	3.3 V ±2%	Pass
Output ripple	$I_{OUT} = 2\,\text{A}$	24.6 mV pk-pk	<33 mV	Pass
Quiescent current	Burst mode, no load	21 µA	<25 µA	Pass
Load transient (0-2 A)	1 A/µs step	1.8% deviation	<2%	Pass

Table 4: Summary of measured bench performance.

8 PCB Layout Recommendations

- Minimize the area of the high-frequency loop formed by C_{IN}, U1, and the power ground return; place C_{IN} as close as possible to the VIN and GND pins of U1.
- Route the SW node as a short, wide trace directly to L_1; avoid routing SW beneath sensitive analog circuitry.
- Place R_1 and R_2 close to the FB pin and route the FB trace away from SW and L_1 to avoid noise coupling into the feedback loop.
- Use a solid ground plane on an inner layer with multiple vias stitching U1's thermal pad to the plane for heat spreading.
- Keep C_{OUT} close to the load connector to minimize output trace inductance and improve transient response.
- Provide a dedicated thermal relief and generous copper pour on the VIN and SW planes to aid conducted heat dissipation.

> **⚠ CAUTION:** Excessive loop area in the C_{IN}–U1–ground path is the most common root cause of switch-node ringing and CISPR 32 conducted-emission failures observed in early prototypes. Verify loop area against Figure 1 before release to production.

9 Reference Design Checklist

☐ Confirm V_{IN} is present and within 4.5 V–5.5 V at the input connector before enabling the board.

☐ Verify the EN pin transitions high and V_{OUT} rises to 3.3 V $\pm 2\%$ within 5 ms of enable.

☐ Measure output ripple with an AC-coupled scope probe; confirm $<$33 mV peak-to-peak at full load.

☐ Record efficiency at 0.2 A, 1 A, and 2 A load points; confirm $>$90% at 1 A.

☐ Perform a 0 A-to-2 A load transient test; confirm V_{OUT} recovers within 2% in under 50 µs.

☐ Capture a thermal image at 2 A, 25°C ambient, after 10 minutes; confirm the U1 case temperature is below 105°C.

☐ Verify the FB trace is routed away from the SW node and L_1 per Section 8.

☐ Confirm the silkscreen revision marking matches the assembly drawing revision (Rev. C).

☐ Run a conducted-emissions pre-scan and compare against the CISPR 32 Class B limit.

☐ Archive all test data and sign off in the engineering change order (ECO) system.

References

1. Solstice Semiconductor, "SSC61830 – 5.5 V Input, 2 A Synchronous Step-Down Converter," Datasheet Rev. 4, 2026.
2. Solstice Semiconductor, "AN-2205: PCB Layout Guidelines for High-Efficiency DC-DC Converters," Application Note, 2025.
3. CISPR 32:2015, "Electromagnetic compatibility of multimedia equipment – Emission requirements."

