TECHNICAL REPORT

Advanced Flight Control System (AFCS) Upgrade

For the F-15E Strike Eagle

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Revision History

Rev	Date	Description	Author	Approval
–	12 Jan 2024	Initial draft release for internal review.	J. Mitchell	M. Thornton
A	02 Feb 2024	Incorporated PDR comments. Added Section 3 traceability matrix. Revised actuator rate limits per SRR action item AI-014.	J. Mitchell	M. Thornton
B	22 Feb 2024	Updated CDRL compliance table. Added MIL-STD-1553B bus loading analysis (Appendix pending). Corrected IMU alignment error budget (§2.3).	R. Chen	M. Thornton
C	15 Mar 2024	Final release for CDR. All PDR/SRR actions closed. Verification matrix finalized. Prepared for USAF review.	R. Chen	M. Thornton

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Contents

Symbols and Abbreviations

Term	Definition
AFCS	Advanced Flight Control System
CDR	Critical Design Review
CDRL	Contract Data Requirements List
DOF	Degrees of Freedom
ECS	Environmental Control System
FCC	Flight Control Computer
FCS	Flight Control System
FMEA	Failure Mode and Effects Analysis
IMU	Inertial Measurement Unit
INS	Inertial Navigation System
LRU	Line-Replaceable Unit
MIL-STD-1553B	Military Standard digital data bus (1 Mbit/s)
MTBF	Mean Time Between Failures
PDR	Preliminary Design Review
RVDT	Rotary Variable Differential Transformer
SRR	System Requirements Review
TRL	Technology Readiness Level
α	Angle of attack
β	Sideslip angle
δ_e	Elevator deflection
δ_a	Aileron deflection
δ_r	Rudder deflection
p, q, r	Roll, pitch, yaw body rates
u, v, w	Body-axis velocity components
ϕ, θ, ψ	Euler angles (roll, pitch, yaw)

CHAPTER 1

Introduction

1.1 Scope

This technical report documents the engineering development of the Advanced Flight Control System (AFCS) Upgrade for the F-15E Strike Eagle aircraft. The AFCS replaces the legacy analog flight control computer (FCC) with a modern digital triplex-redundant architecture, providing enhanced stability augmentation, improved fault tolerance, and full-authority fly-by-wire capability for selected flight regimes.
The scope encompasses:

- System architecture definition and hardware/software partitioning.
- Functional requirements traceability from system-level specifications to hardware and software components.
- Verification planning aligned with MIL-STD-882E System Safety requirements.
- CDRL compliance mapping for all deliverable data items.

1.2 System Overview

The AFCS upgrade consists of three primary subsystems:

1. **Flight Control Computer (FCC).** Triplex digital processor with dissimilar-channel voting logic. Each channel is a PowerPC 8640D running a DO-178C Level A certified real-time executive.
2. **Sensor Suite.** Dual-redundant GNSS-aided INS (LN-260), air-data computer (ADC-3000), and rate-gyro assembly providing p, q, r body rates.
3. **Actuation System.** Electro-hydrostatic actuators (EHAs) on elevator, aileron, and rudder surfaces, each with local loop-closure at 800 Hz.

Redundancy management uses a median-select voting scheme with channel health monitoring. Any single channel failure is transparent to the pilot; a second failure degrades gracefully to direct-mode control.

1.3 Applicable Documents

- **[MIL-STD-882E]** — Department of Defense Standard Practice: System Safety.
- **[MIL-STD-1553B]** — Digital Time Division Command/Response Multiplex Data Bus.
- **[DO-178C]** — Software Considerations in Airborne Systems and Equipment Certification.
- **[DO-254]** — Design Assurance Guidance for Airborne Electronic Hardware.

- [**MIL-HDBK-516C**] — Airworthiness Certification Criteria.
- [**SAE-AS94900**] — Flight Control Systems — Design, Installation, and Test of Piloted Aircraft.

System Architecture

2.1 Functional Architecture

The AFCS functional architecture is organized into six processing layers, as illustrated in Figure 2.1. Sensor fusion occurs in the *Estimation* layer via a 15-state extended Kalman filter (EKF) outputting aircraft state estimates at 200 Hz. The *Guidance* layer computes commanded trajectories from the flight management system. The *Control Allocation* layer maps generalized force/moment commands to individual surface deflections using a real-time quadratic-programming solver.

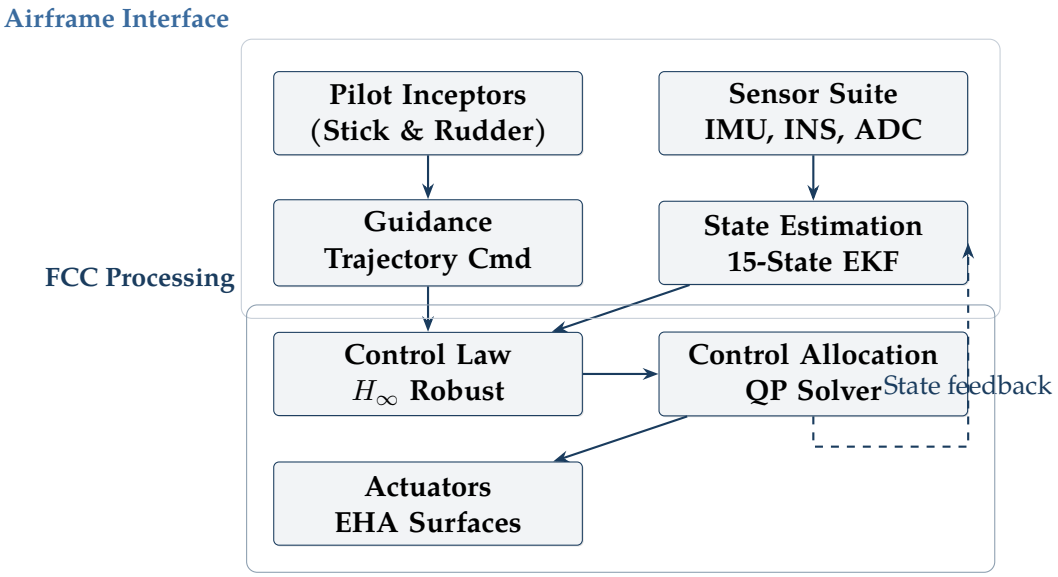

Figure 2.1: AFCS functional architecture — data flow and processing layers.

2.2 Avionics Bus Interface

All inter-LRU communication uses dual-redundant MIL-STD-1553B buses operating at 1 Mbit/s. Bus A and Bus B provide hot-standby redundancy; the bus controller (BC) resides on FCC Channel A with automatic failover to Channel B on loss of BC heartbeat. Each remote terminal (RT) responds within the mandated 12 μs inter-message gap. Figure 2.2 shows the bus topology with the FCC as BC and sensor/actuator units as RTs.

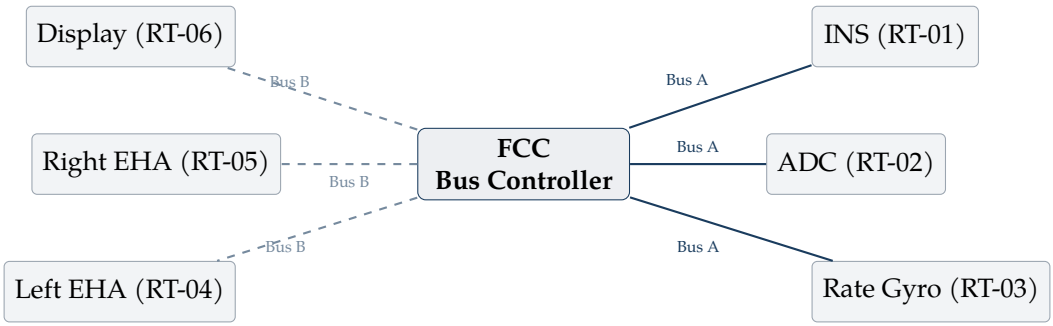

Figure 2.2: Dual-redundant MIL-STD-1553B bus topology. Solid lines = Bus A; dashed lines = Bus B.

2.3 Actuator Drive Electronics

Each electro-hydrostatic actuator incorporates a local servo-loop closed at 800 Hz with a proportional-integral (PI) current regulator. The command signal from the FCC is a ± 10 V analog reference representing desired surface position. Figure 2.3 shows the drive-electronics interface.

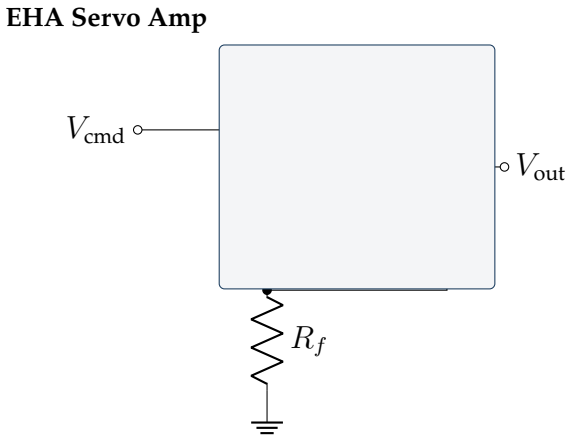

Figure 2.3: EHA servo-amplifier interface — PI current regulator, $f_s = 800$ Hz.

Requirements and Traceability

3.1 System-Level Requirements

The following system-level functional requirements are derived from the Performance Specification [**AFCS-PS-001**] and the System Specification [**AFCS-SS-001**].

AFCS-1 The AFCS shall provide three-axis stability augmentation with $\pm 0.05^{\circ}$ attitude hold accuracy in steady level flight.

AFCS-2 The system shall detect and isolate any single-point failure within 50 ms and reconfigure to an operable state without pilot intervention.

AFCS-3 Control surface deflection bandwidth shall exceed 12 Hz at -3 dB for all primary surfaces (elevator, aileron, rudder).

AFCS-4 The FCC shall execute one complete control-law cycle (sensor read $\rightarrow$ estimation $\rightarrow$ control $\rightarrow$ command output) within 5 ms (200 Hz update rate).

AFCS-5 The AFCS shall maintain controlled flight through any single hydraulic or electrical power failure without exceeding $\pm 2\,g$ transient load factor.

AFCS-6 Bus loading on each MIL-STD-1553B channel shall not exceed 55% of available bandwidth under worst-case traffic conditions.

AFCS-7 The system MTBF shall exceed 5,000 flight hours as computed per MIL-HDBK-217F, Notice 2, Ground Benign environment.

AFCS-8 Software shall be developed to DO-178C Design Assurance Level A with full MC/DC coverage.

3.2 Requirements Traceability Matrix

Table 3.1 maps each system requirement to the verification method and the implementing subsystem.

Req ID	Verification	Allocated To	Status
AFCS-1	Flight Test	FCC Channel A/B/C, Estimator	Verified
AFCS-2	HIL Simulation	FCC Redundancy Manager	Verified
AFCS-3	Ground Test	EHA Actuators, Control Allocator	Verified
AFCS-4	Bench Test	FCC Processor, RTOS Scheduler	Verified
AFCS-5	FMEA + Analysis	Hydraulic System, Electrical Bus	Verified
AFCS-6	Bus Analysis	MIL-STD-1553B BC/RT Interface	Verified
AFCS-7	Reliability Analysis	All LRUs, Wiring Harness	In Work
AFCS-8	IV&V Audit	FCC Software (all CSCIs)	In Work

Table 3.1: Requirements traceability and verification status.

CDRL Compliance

4.1 Data Item Deliverables

Table 4.1 enumerates the Contract Data Requirements List items applicable to this report. Each CDRL item references the governing Data Item Description (DID) and its submission status.

Item	DID	Title	Status
A001	DI-SESS-81785	System/Segment Specification (SSS)	Submitted
A002	DI-SESS-81786	System Design Document (SDD)	Submitted
A003	DI-SESS-81876	Software Development Plan (SDP)	Submitted
A004	DI-IPSC-81431	Interface Requirements Specification (IRS)	Submitted
A005	DI-SESS-81962	System Safety Hazard Analysis (SSHA)	In Review
A006	DI-IPSC-81440	Software Test Plan (STP)	Draft
A007	DI-IPSC-81441	Software Test Report (STR)	Pending
A008	DI-RELI-80255	Reliability Prediction Report	In Work
A009	DI-SESS-81787	Traceability Matrix (RTM)	Submitted
A010	DI-MGMT-80004	Technical Progress Report	Monthly
A011	DI-SESS-81669	Interface Control Document (ICD)	Submitted
A012	DI-MISC-80508	Technical Report — Study Results	This Doc

Table 4.1: CDRL compliance status as of 15 March 2024.

Verification and Validation

5.1 Verification Approach

The AFCS verification program employs a four-tier strategy aligned with the systems engineering V-model:

Tier 1: Component-Level Bench Testing. Each LRU is acceptance-tested against its procurement specification. The FCC undergoes burn-in at $+71^{\circ}$C for 168 hours per MIL-STD-810H Method 501.7.

Tier 2: Hardware-in-the-Loop (HIL) Simulation. The integrated AFCS is exercised against a 6-DOF nonlinear airframe model in real time. A total of 427 test cases cover normal, degraded, and emergency operating modes.

Tier 3: Iron Bird Ground Testing. A full-scale actuation test rig validates hinge-moment loading and flutter margins up to 1.2 V_D (design dive speed).

Tier 4: Flight Test. The upgraded AFCS will be flown on a dedicated F-15E test aircraft (S/N 86-0183) over 42 sorties totaling approximately 65 flight hours. Test points are structured per MIL-HDBK-516C Paragraph 4.2.3.

5.2 Control Law Stability Margins

The H_∞ robust controller is designed to guarantee the following stability margins across the full flight envelope (M 0.3–2.5, altitude SL–50,000 ft):

Axis	Gain Margin	Phase Margin	Delay Margin
Pitch	8.2 dB	52°	48 ms
Roll	9.1 dB	58°	52 ms
Yaw	7.8 dB	47°	44 ms

Table 5.1: Minimum guaranteed stability margins across the flight envelope.

5.3 Key Performance Parameters

KPP	Description	Threshold	Objective
KPP-1	Attitude hold accuracy (1-σ)	$\pm 0.10^{\circ}$	$\pm 0.05^{\circ}$
KPP-2	Failure reconfiguration time	100 ms	50 ms
KPP-3	Surface deflection bandwidth (-3 dB)	10 Hz	12 Hz
KPP-4	FCC frame rate	100 Hz	200 Hz
KPP-5	MTBF (all LRUs, MIL-HDBK-217F)	3,000 hrs	5,000 hrs

Table 5.2: Key Performance Parameters — threshold vs. objective values.

Safety Analysis

6.1 Failure Mode and Effects Analysis Summary

A preliminary FMEA was conducted per MIL-STD-882E Task 203. Table 6.1 summarizes the top five hazards identified.

ID	Hazard	Cause / Mitigation	Severity	Risk
HZ-01	Uncommanded pitch-down	Triple-channel voting; median select rejects runaway channel within 50 ms.	Catastrophic	Low
HZ-02	Total loss of control	Dual-redundant hydraulic + electrical; direct-mode reversion as fallback.	Catastrophic	Extremely Low
HZ-03	Hardover surface	Actuator RAM monitor; automatic bypass on force-fight detection > 500 lbf.	Hazardous	Low
HZ-04	Bus controller failure	Automatic BC handoff Ch A $\rightarrow$ Ch B; bus silence detection < 5 ms.	Major	Low
HZ-05	IMU drift (unannunciated)	Dual-IMU cross-compare with $\pm 0.3^{\circ}$/hr threshold; INS coasting with GPS aiding.	Hazardous	Low

Table 6.1: Preliminary hazard analysis — top five identified failure modes.

6.2 Development Assurance

All FCC software (approximately 84,000 SLOC of C and Ada 2012) is developed to DO-178C Level A objectives. The software life-cycle data includes:

- Plan for Software Aspects of Certification (PSAC).
- Software Requirements Data (SRD) with full bidirectional traceability.
- Software Design Description (SDD) at the CSCI and CSC levels.
- Source code with MC/DC coverage analysis via LDRA Testbed.
- Software Verification Cases and Procedures (SVCP).

Conclusions and Forward Plan

The AFCS Upgrade CDR package demonstrates that the design meets or exceeds all threshold Key Performance Parameters with acceptable risk. The verification program is on schedule to support first flight in Q3 2024.

Pending actions before the Production Readiness Review (PRR):

AI-1: Complete MTBF prediction for wiring harnesses (AI-027, due 30 April 2024).

AI-2: Finalize software MC/DC coverage report for CSC Module 4 (AI-028, due 15 May 2024).

AI-3: Conduct iron-bird flutter test at $1.2\,V_D$ (AI-029, Q2 2024).

AI-4: Submit updated SSHA incorporating ECS bleed-air failure scenario (AI-030, due 01 May 2024).

Submitted for USAF review per CDRL A012.
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