Hardware Verification & Validation Test Plan

System Level Testing for Nimbus-5 Edge SoC

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Abstract

This document defines the system-level Hardware Verification & Validation (V&V) Test Plan for the **Nimbus-5 Edge System-on-Chip (SoC)**. It establishes the testing framework, hardware instrumentation setup, test vector stimuli, and verification protocols for validating chip-level logic, high-speed peripheral interfaces, and board-level signal integrity. This plan provides the formal methodology for QA and test engineers to execute physical layer testing, JTAG boundary scan, logical pattern validation, and systematic defect reporting. Compliance with the criteria defined herein is mandatory for production release certification of the Nimbus-5 platform.

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1 Introduction

1.1 System Overview

The Nimbus-5 Edge System-on-Chip (SoC) is a high-performance, low-power processing platform designed for edge artificial intelligence and IoT gateway deployments. Developed by Apex Technologies, the Nimbus-5 incorporates an octa-core RISC-V application processor, a dedicated neural processing unit (NPU), and high-speed interfaces including PCIe Gen 3, USB 3.2, Dual Gigabit Ethernet, and LPDDR4 memory controllers.

To ensure the commercial viability and reliability of the Nimbus-5 platform, this hardware verification and validation (V&V) document outlines the system-level testing requirements at both the silicon (chip) and board level. All testing procedures are conducted by Vertex Validation Engineering and approved by Synapse QA Engineering.

1.2 Scope of Document

This document describes the validation flow, testing environments, instrumentation setups, and logic analyzer configurations required to verify the hardware implementation of Nimbus-5. Specifically, it covers:

- System-level board bring-up validation.
- High-speed digital interface signal integrity.
- Test vector execution for memory and communications controllers.
- Defect categorization and reporting protocols for validation engineers.

1.3 Referenced Documents

The validation procedures in this document are aligned with the technical standards and project specifications listed in Table 1.

Document Code	Title	Publisher
IEEE Std 1149.1-2013	Standard Test Access Port and Boundary-Scan Architecture	IEEE Computer Society
APX-N5-DS-v1.4	Nimbus-5 SoC Hardware Data Sheet	Apex Technologies
PCI-SIG Gen3 v1.0	PCI Express Base Specification Revision 3.0	PCI-SIG Consortium
JESD209-4B	Low Power Double Data Rate 4 (LPDDR4) Standard	JEDEC Solid State

Table 1: Reference specifications and standards.

1.4 Glossary of Terms

- **DUT**: Device Under Test.
- **HUT**: Hardware Under Test.
- **LA**: Logic Analyzer.
- **V&V**: Verification and Validation.
- **JTAG**: Joint Test Action Group.

2 Test Environment & Setup

2.1 Physical Test Environment

All hardware verification must be conducted within an Electrostatic Discharge (ESD) protected validation laboratory. The ambient temperature of the testing room must be regulated to $22^{\circ}\text{C} \pm 3^{\circ}\text{C}$ with relative humidity kept between 30% and 60% to ensure repeatable thermal baselines for active chip operations. Nexa-compliant electrostatic wrist straps and grounded dissipative table mats are mandatory for all test operators.

2.2 Hardware Instrumentation Setup

The hardware validation setup integrates logic analysis, signal capture, power monitoring, and diagnostic software execution. The key physical instruments utilized in this plan are:

- **Apex LogicPro 128-Channel Logic Analyzer**: Configured to sample digital signals up to 2.5 GS/s, enabling capture of transient timing faults on high-speed buses.
- **Vertex DSO 4 GHz Oscilloscope**: Equipped with active differential probes to assess analog signal integrity and eye diagrams.
- **Synapse Programmable Power Supply**: Delivers stable, low-noise DC power rails (0.9V, 1.2V, 1.8V, and 3.3V) with precision current-sensing.
- **Host Controller PC**: Runs the Apex Test Orchestrator suite, generating test patterns, configuring instruments, and logging validation outputs.

Figure 1 illustrates the interconnect topology of the test environment.

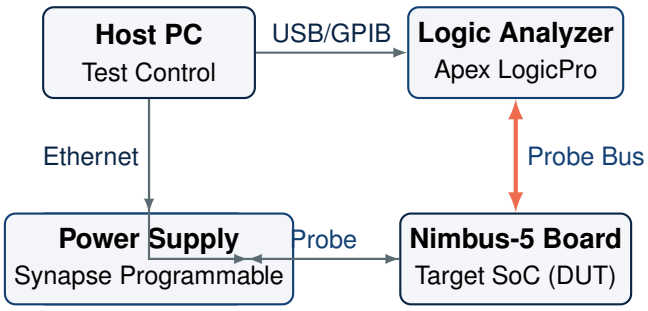

Figure 1: System test setup and instrument connections.

2.3 Logic Analyzer Configuration

The Apex LogicPro logic analyzer must be calibrated before executing test cycles. The default configuration parameters for data capture are defined as follows:

- **Sampling Mode**: State mode synchronized to the DUT system clock up to 400 MHz, or asynchronous timing mode at 2.5 GS/s.
- **Trigger Condition**: Configured to trigger on JTAG state transition sequence (TMS low to high) or PCIe packet framing errors.
- **Signal Mapping**: Pre-configured template `nimbus5_evb_v2.xml` mapping the 128 physical probe channels to JTAG, SPI, I2C, and DDR controller control lines.

3 Verification Procedures & Test Vectors

3.1 Test Vector Stimuli

To validate chip-level logical states and bus communication integrity, verification engineers must load and execute standard test vectors. The digital patterns verify command decoding, timing margins, and operational reliability. Table 2 contains the core test vector sequences for high-speed bus interfaces.

Vector ID	Interface	Stimulus Pattern (Hex)	Expected Output
VEC-001	JTAG	`0x3F0A1E4B8C9D0E1F`	`0xAA55AA55`
VEC-002	SPI	`0xAA5500FF55AAFF00`	`0x55AAFF0055AA00FF`
VEC-003	I2C	`0x70 [W] 0x02 0x5A`	ACK + Register Write Success
VEC-004	PCIe	Link training sequence (TS1/TS2)	Link state L0 active

Table 2: High-speed interface verification test vectors.

3.2 Step-by-Step Test Execution

Verification engineers must perform the testing protocol in sequence. The general testing steps are:

1. **Power-up Sequence Validation**: Ensure that the programmable power supply triggers voltage rails in order ($3.3\text{V} \rightarrow 1.8\text{V} \rightarrow 1.2\text{V} \rightarrow 0.9\text{V}$). Check current draw limits to confirm no short circuits.
2. **Clock Initialization Verification**: Monitor the $25\,\text{MHz}$ oscillator. Check phase lock loop (PLL) registers to ensure core clock reaches $1.2\,\text{GHz}$ without frequency jitter.
3. **Boundary Scan Validation**: Verify logic pathway continuity using JTAG boundary scan commands.
4. **High-speed Interface Validation**: Execute high-speed data bursts on DDR and PCIe channels. Log error rates and eye diagrams on the oscilloscope.

3.3 Pass/Fail Criteria

The verification tests are marked pass or fail based on strict technical thresholds:

- **Signal Integrity**: Rise/fall times must be $\leq 120\,\text{ps}$ for PCIe lanes, and eye-opening width must exceed 70% of unit interval (UI).
- **JTAG Operation**: TAP controller must return IDCODE matching the Nimbus-5 signature register `0x0A5C2043`.
- **Bit Error Rate (BER)**: PCIe link must run error-free for a minimum of 10^9 bits under thermal stress test.

⚠ Interface Failure Protocol

If the PCIe link fails to achieve L0 state after five subsequent re-train loops, power down the DUT immediately. Check if pin probes on TX/RX lines are introducing capacitive load distortion ($\geq 1.5\,\text{pF}$).

4 Defect Reporting & Issue Tracking

4.1 Defect Classification Workflow

When a validation test fails, the testing engineer must log the issue. Defects are tracked dynamically and undergo verification checks before resolution. The lifecycle of a defect is:

1. **Identification**: Validation engineer observes a violation of pass/fail criteria.

2. **Filing**: Bug report is created, containing hardware revision, logic analyzer traces, and test vector ID.
3. **Triage**: Hardware design team determines severity and assigns to a resolution owner.
4. **Mitigation**: Design changes are proposed (e.g., PCB trace impedance tuning or firmware register adjustments).
5. **Verification**: The test is rerun on the mitigated board to confirm pass criteria are met.

4.2 Defect Severity Definition

Defects are classified into four severity levels. Table 3 outlines the classification matrix.

Severity Level	Systemic Impact	Resolution Deadline
Critical	System crash, permanent hardware damage, or boot path failure.	Immediate (stop line validation)
Major	High-speed interface link training fails, or memory corruption.	48 hours
Minor	Minor functional issue with a software bypass (e.g., I2C clock stretch bypass).	7 business days
Cosmetic	Document inconsistencies, GPIO LED timing mismatch.	Next revision candidate

Table 3: Defect severity classification matrix.

4.3 Sample Defect Log Entry

Below is a sample log entry for an actual verification defect.

Listing 1: Defect report log entry (DF-2026-N5-042).

```
[DEFECT LOG]
ID: DF-2026-N5-042
Severity: Major
Component: PCIe Gen 3 Controller
Revision: Apex EVB v2.1
DUT Serial: SN-49201-A
Tester: Marcus Vance (QA Engineer)

Description:
During VEC-004 test vector execution, PCIe lanes 0-3 successfully negotiate to L0 state, but lane
     4 reports intermittent framing error during active RX states.

Root Cause:
PCB trace length matching variance on lane 4 RX pair exceeds 2.5 mil tolerance limit, resulting
    in dynamic skew under peak load.

Mitigation:
1. Re-route RX differential pair in PCB revision v2.2.
2. For v2.1 board testing, apply soft-register offset PCIe_RX_SKEW_CTRL (0x0F48) to delay clock
    phase by 40 ps on lane 4.

Verification Status:
Pass (Verified under active skew control firmware patch).
```

References

[1] Apex Technologies Design Group. *Nimbus-5 Edge SoC Hardware Design Specification*. Apex Technologies, v2.4 edition, 2026. Confidential Technical Document.

[2] IEEE Computer Society. Ieee standard test access port and boundary-scan architecture. *IEEE Std 1149.1-2013*, pages 1–447, 2013.

[3] Howard W. Johnson and Martin Graham. *High-Speed Digital Design: A Handbook of Black Magic*. Prentice Hall PTR, Upper Saddle River, NJ, 1993.

[4] Neil H. E. Weste and David Money Harris. *CMOS VLSI Design: A Circuits and Systems Perspective*. Pearson Education, Boston, MA, 2018.