Priya Nair

VLSI Design Engineer | RTL | ASIC Implementation

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Professional Summary

VLSI design engineer with 7+ years of experience delivering low-power digital IP and SoC blocks from microarchitecture and RTL through synthesis, timing closure, and signoff. Proven record on 5–16 nm designs spanning coherent interconnect, memory controllers, and high-speed peripherals. Combines strong SystemVerilog design fundamentals with hands-on static timing analysis, CDC/RDC, formal lint, UPF, and close collaboration across verification and physical-design teams.

Technical Skills

RTL & Architecture: SystemVerilog, Verilog, synthesizable RTL, finite-state machines, pipelining, clock/reset design, AMBA AXI4/APB, cache-coherent fabrics
ASIC Flow: Design Compiler, Fusion Compiler, Genus, PrimeTime, Tempus, synthesis, SDC, STA, timing closure, LEC, ECOs, DFT collaboration
Quality & Low Power: SpyGlass lint/CDC/RDC, Questa CDC, Formality, Conformal, UPF, clock gating, power gating, multi-voltage design
Verification & Automation: SystemVerilog Assertions, UVM familiarity, VCS, Xcelium, Verdi, Python, Tcl, Perl, Make, Git, Linux, Jenkins

Professional Experience

Senior VLSI Design Engineer — **Mar 2022 – Present**
Orion Semiconductor — Austin, TX

- Owned microarchitecture and RTL delivery for a 5 nm AXI4 interconnect subsystem with 12 initiators and 18 targets, meeting a 1.4 GHz performance target across signoff corners.
- Added transaction pipelining, arbitration tuning, and critical-path restructuring that improved worst negative slack by 180 ps while holding area growth below 1.8%.
- Defined UPF intent for three voltage domains and partnered with physical design to close isolation, retention, and level-shifter checks, reducing subsystem dynamic power by 21%.
- Drove lint, CDC/RDC, LEC, and synthesis signoff; resolved 140+ structural and clock-domain issues before integration and achieved zero design-owned escapes at tapeout.
- Built Python and Tcl dashboards for PPA and timing-regression triage, shortening weekly analysis from six engineer-hours to under 30 minutes.

VLSI Design Engineer II — **Jul 2019 – Feb 2022**
Silica Microsystems — San Jose, CA

- Designed command scheduling, refresh, and error-handling RTL for a 7 nm LPDDR4X controller deployed in two mobile SoCs with first-pass silicon success.
- Closed block-level timing at 1.2 GHz by refining multicycle/false-path constraints and retiming control logic, recovering 95 ps of setup margin at the slow corner.
- Implemented clock-gating and activity-driven RTL changes that cut block dynamic power 17% with no measurable performance loss.
- Collaborated with UVM verification on assertions, coverage gaps, and failure debug; increased functional coverage from 91% to 98.7% before design freeze.

ASIC Design Engineer — **Jun 2017 – Jun 2019**
Vector Logic Labs — Raleigh, NC

- Developed and integrated APB peripherals, DMA control logic, interrupt aggregation, and reset sequencing for 16 nm networking ASICs.
- Automated synthesis, lint, and equivalence-check flows for 20+ blocks, cutting turnaround time 35% and standardizing waiver tracking across the team.
- Supported scan insertion and ATPG closure by repairing test-mode timing and controllability issues, contributing to 99.3% stuck-at fault coverage.

Selected Engineering Project

Parameterizable RISC-V RV32IM Five-Stage Core — SystemVerilog, SVA, Python

- Implemented forwarding, hazard detection, branch recovery, CSR support, and configurable instruction/data caches; verified ISA behavior with directed and constrained-random tests.
- Synthesized the core in an open 130 nm flow at 100 MHz and published reproducible RTL, assertions, testbench, and PPA reports at github.com/priyanair-rtl/rv32-pipeline.

Education

M.S., Electrical and Computer Engineering — 2015 – 2017
North Carolina State University, Raleigh, NC — GPA: 3.8/4.0

B.Tech., Electronics and Communication Engineering — 2011 – 2015
National Institute of Technology Karnataka, Surathkal, India — Graduated with Distinction